

## AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph before "Background of the Invention" as follows:

This application is a continuation of U.S. Application Serial No. 10/230,079 filed on August 29, 2002, now U.S. Patent No. 6,744,084 issued on June 1, 2004, the disclosure of which is incorporated by reference herein.

Please amend paragraph [0020] on page 4 of the specification as follows:

[0020] Referring now to the drawings, where like elements are designated by like reference numerals, Figures 2-7 illustrate an exemplary embodiment of a method of forming a two-transistor CMOS pixel 100 (Figure 7) having a buried reset region 199 formed in contact with and adjacent a charge collection region 126 of a photodiode 188, which also has a region 124 over region 126 which is of complementary conductivity type to region 126. The reset region 199 acts as an extension of charge collection region 126 of photodiode 188 and also functions to reset the extended charge collection region. As explained in detail below, the reset region 199 (Figure 7) is formed by implanting dopants of a first conductivity, for example n-type, and at a first dopant concentration in a substrate 110, which has a region or well 120 of a second conductivity type, for example p-type. The buried reset channel 199 (Figure 7) contacts with the charge collection region 126 of the first conductivity type, for example n-type, and is provided with a contact region 177 (Figure 7) of the first conductivity type, for example n-type. The contact region 177 is further connected by a conductor 137 to a gate of a source follower transistor 136, the output of which (drain 140) is connected to a row select transistor 138.

Please amend paragraph [0043] of the specification as follows:

[0043] The pixel is also reset before and after signal integration. Referring to Figures 7 and 8 during reset, the normally high voltage Vpd coupled to capacitor 171 from reset signal source 176 is pulsed low, e.g., to zero volts. This causes the charge within reset region 199 to effectively move upwardly in the direction of arrow A such that charges within channel 199 spill over barrier 147 into n+ region 142 which is connected to Vdd. Thus, charges are ejected from the photodiode region 126 and the reset region 199 and into n+ region 142 connected to Vdd. Vpd is then returned to a high value, for example 3.3 V, allowing charge integration to occur. This integrated charge is then read out in the manner described above. The barrier potential 147 is set to allow an anti-blooming operation to occur when charges collected on capacitor 171 in region 199 exceed the barrier potential [[145]] 147. This excess charge spills over to n+ region 142.

Please amend paragraph [0043] of the specification as follows:

[0047] A processor based system, such as a computer system, for example generally comprises, in addition to a CMOS imager 642 input device, a central processing unit (CPU) 644, for example, a microprocessor, that communicates with one or more input/output (I/O) devices 646 over a bus 652. The CMOS image sensor 642 also communicates with the processor system over bus 652 or over other conventional communication path. The computer system 600 also includes random access memory (RAM) 648, and, in the case of a computer system may include peripheral devices such as a floppy disk drive 654, and a compact disk (CD) ROM drive 656 or a flash memory card [[657]] which also communicate with CPU 644 over the bus 652. It may also be desirable to integrate the processor 644, CMOS image device 642 and memory 648 on a single IC chip.